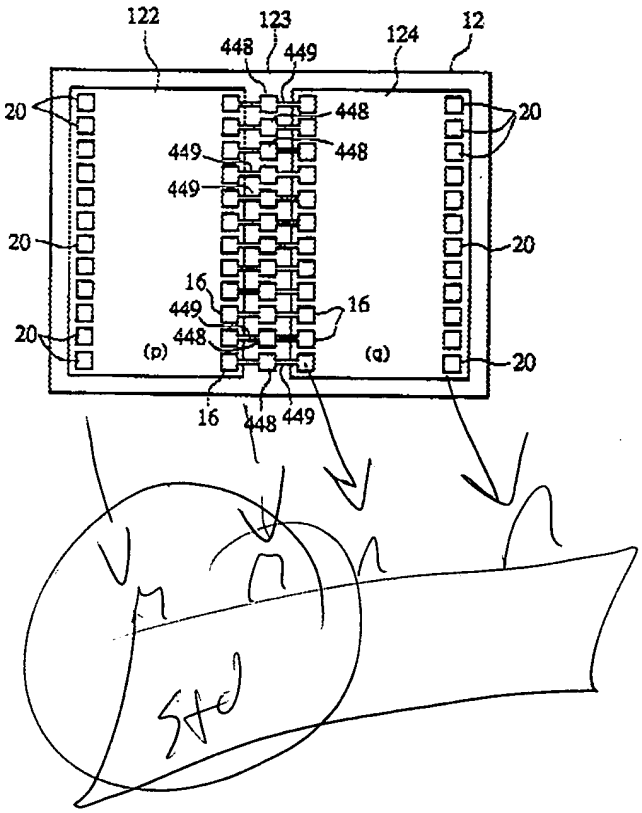
FIG. 21



level L, as shown in FIG. 19. Since there is no decision circuit between the bonding pads P3 and P4, no current flows between the bonding pads P3 and P4. As a result, the product is determined to be not of a normal configuration.

FIG. 20 shows the decision circuit mounted on a reverse semiconductor chip 12. The level setting of pins of the reverse chip 12 is the same as that of the normal chip of FIG. 18. Only the pin arrangement of FIG. 20 is opposite to that of FIG. 18. According to the same operations as those of the normal chip, a current flows between the bonding pads P1 and P2 of the reverse chip.

In this way, the decision circuit for determining a type of a semiconductor device is arranged on a semiconductor IC chip. A probe card to carry out an operation test is made to contact the bonding pads of the IC chip, to determine the type of the IC to be tested. It is not necessary for an inspector to aware of the type of a semiconductor device to be tested, thereby avoiding test errors and defective devices due to the test errors. At a product test, normal and reverse semiconductor devices will be mixed up. It is necessary, therefore, to sort the devices before the test. When the same lead frame is used for normal and reverse semiconductor devices according to the third embodiment of the present invention, it will be difficult to sort the devices after packaging them. In this case, the decision circuit of the fourth embodiment is effective to sort the devices and avoid test errors.

The decision circuit not only determines the type of a device but also a write permit status, a function option, a circuit option, or the number of refresh cycles.

FIG. 21 is a plan view showing a semiconductor device according to the fifth embodiment of the present invention. A semiconductor chip 12 supports a normal IC 122 and a reverse IC 124. The ICs 122 and 124 are each a mirror image of the other. Normal bonding pads 16 are connected to reverse bonding pads 16 through metal wirings 449 and bonding pads 448 formed at the center of the chip 12. The ICs 122 and 124 are each of, for example, 64 megabits. They are connected together to form a double-capacity IC, i.e., a 128-megabit IC. In this way, the fifth embodiment easily forms a double-capacity semiconductor device without newly fabricating a double-capacity mask or executing a new manufacturing process. The fifth embodiment is effective to shorten the development time and reduce the costs of large-capacity semiconductor devices. If the large capacity (double capacity) is not needed, the semiconductor chip 12 of FIG. 21 may be separated into a normal semiconductor chip and a reverse semiconductor chip, each chip being mounted on a separate lead frame, as shown in FIG. 22. Namely, the fifth embodiment can easily increase or decrease the capacity of a semiconductor device by optionally determining a dicing line without changing masks and processing steps. If two pairs of normal and reverse ICs are formed on a single chip as shown in FIG. 23, the capacity will be quadrupled.

Various modifications will become possible for those skilled in the art after receiving the teachings of the present disclosure without departing from the scope thereof.

What is claimed is:

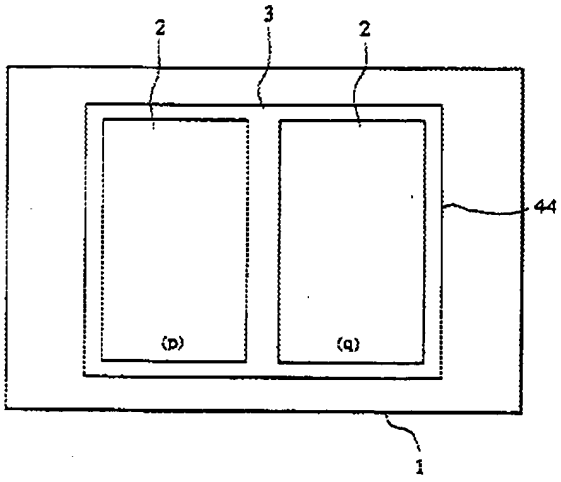
1. A semiconductor device for mounting in a package having a plurality of outer pins, the semiconductor device comprising:

a semiconductor wafer;

a first integrated circuit having a first pattern of elements, a first side and a second side opposing the first side and a first centerline between the first and second sides;

a second integrated circuit having a second pattern of elements, a third side and a fourth side opposing the

FIG. 9



level L_1 as shown in FIG. 19. Since there is no decision circuit between the bonding pads P3 and P4, no current flows between the bonding pads P3 and P4. As a result, the product is determined to be not of a normal configuration.

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Various modifications will become possible for those skilled in the art after receiving the teachings of the present disclosure without departing from the scope thereof.

What is claimed is:

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a second integrated circuit having a second pattern of elements, a third side and a fourth side opposing the

FIG. 19

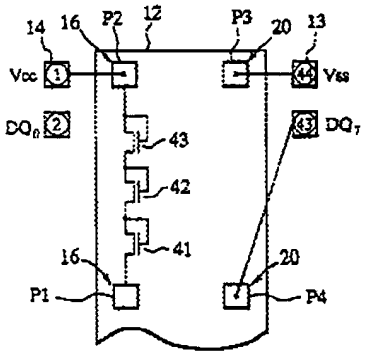
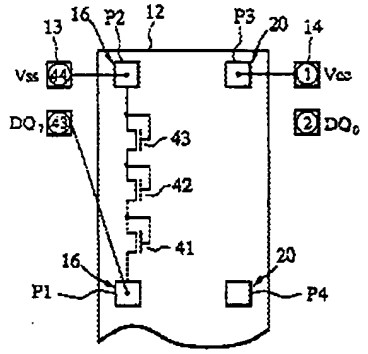


FIG. 20



wafer, only one manufacturing process is sufficient. According to the present invention, all IC patterns are subjected to the same misalignment in the mask and shape fluctuations in the manufacturing process, so that lot-to-lot variations are cancelled and manufacturing time is shortened. According to the present invention, a reverse pattern may be an upside-down mirror image, instead of a right and left mirror image, of a normal pattern.

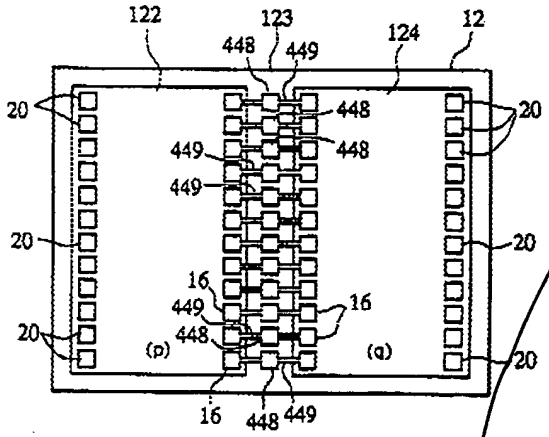
FIG. 12 shows a semiconductor wafer on which IC patterns are sequentially exposed by a stepper with use of the photomask (reticle) of FIG. 9. There are normal IC patterns p and reverse IC patterns q. The reverse IC pattern q is a mirror image of the normal IC pattern p. Four pairs of normal and reverse IC patterns are alternately arranged in each of four rows on the semiconductor wafer. The arrangement of FIG. 12 is only an example. The number of pairs of normal and reverse IC patterns on a wafer is determined according to the area of the wafer and the exposing area of a stepper. The number of IC patterns in a mask also determines the total number of IC patterns on a wafer, as shown in FIGS. 10 and 11. The number of IC patterns is properly determined according to requirements. In FIGS. 9 to 11, a normal IC pattern and a reverse IC pattern forms a pair so that the total number of IC patterns is even. It is possible to employ a mask including an odd number of IC patterns. More normal products are needed in the market than reverse products, so that more normal IC patterns may be formed than reverse IC patterns on a wafer. For example, a mask having two normal IC patterns and a reverse IC pattern may be used to expose a wafer by a stepper.

Although the above explanation is based on photolithography employing a photomask or a reticle, the present invention is also applicable to electron beam exposure or X-ray exposure, or even a direct writing method without a mask or a reticle. In any case, the present invention forms at least a pair of normal and reverse IC patterns each being a mirror image of the other on a semiconductor wafer.

FIG. 13 shows a photomask or a reticle according to the second embodiment of the present invention. The mask includes a normal IC pattern, a reverse IC pattern, and a test circuit pattern. The test circuit pattern is used to form a test circuit that carries out, for example, a reliability test on the normal and reverse ICs. FIG. 14 shows only the metal wirings around the test circuit. The test circuit area 4 is used to form the test circuit 444, a connection terminal 445 for supplying an external control signal to the test circuit 444, and an internal signal output terminal 446 used to monitor test signals. The normal and reverse ICs are symmetrical with respect to the test circuit area 4, so that the ICs are easily connected to the test circuit through metal wirings 449. Unlike the prior art that provides each of normal and reverse ICs with a test circuit, the second embodiment of the present invention lets two, four, eight, or more ICs share a test circuit, thereby increasing the effective area of each chip and the integration of a semiconductor product.

FIGS. 15A and 15B show a probe card for testing a semiconductor wafer having ICs according to the first embodiment of FIGS. 8 and 9. The positions of I/O terminals of a normal IC are not identical to those of a reverse IC. Accordingly, the prior art prepares a probe card for testing normal ICs and a probe card for testing reverse ICs. The probe card for normal ICs are not applicable to reverse ones, and the probe card for reverse ICs are not applicable to normal ones. On the other hand, the probe card of FIGS. 15A and 15B according to the present invention has normal test terminals p and reverse test terminals q, to simultaneously test normal and reverse ICs. The probe card has a disk-like

FIG. 21



respective one of said plurality of outer pins, the bonding pads being symmetrically arranged with respect to said first and second centerlines along said first and second opposing sides and wholly outside of said scribe line area, and said first and second integrated circuits and said scribe line area are formed on said semiconductor wafer.

4. The semiconductor device of claim 3, wherein each of said first and second patterns include a decision circuit to determine whether a respective integrated circuit is said first integrated circuit or said second integrated circuit.

5. The semiconductor device of claim 3, wherein selected bonding pads in each of said first and second integrated circuits are connected to each other through metal wirings formed on said scribe line area.

6. A semiconductor device comprising:

a first package having first external I/O terminals, a first bottom surface and a first integrated circuit having a first pattern of elements and first opposing sides;

a second package having second external I/O terminals, a second bottom surface and a second integrated circuit having a second pattern of elements and second opposing sides, wherein said second pattern is a mirror image of said first pattern, and wherein said first and second patterns each include a plurality of bonding pads respectively arranged along said first and second opposing sides; and

a circuit board for mounting said first and second packages, the circuit board having first and second surfaces,

wherein said first package is mounted on the first surface of said circuit board and said second package is mounted on the second surface of said circuit board, and wherein said first bottom surface faces said second bottom surface.

7. The semiconductor device of claim 6, including: